REMARKS

Claims 1-20 are pending in the application.

Claims 1-20 have been rejected.

Claims 1, 4, 7, and 14 have been amended as set forth herein.

Claims 1-20 remain pending in this application.

Reconsideration of the claims is respectfully requested. The Applicant makes the aforementioned amendments and subsequent arguments to place this application in condition for allowance. Alternatively, the Applicant makes these amendments and offer these arguments to properly frame the issues for appeal.

I. CLAIM REJECTIONS -- 35 U.S.C. § 103

Claims 1-20 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,563,837 to Krishna, et al (hereinafter "*Krishna*"). The Applicant respectfully traverses the rejection.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a prima facie case of obviousness. MPEP § 2142, p. 2100-133 (8th ed. rev. 4, October 2005). Absent such a prima facie case, the Applicant is under no obligation to produce evidence of nonobviousness. *Id.* To establish a *prima facie* case of obviousness, three basic criteria must be met: *Id.* First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to

combine reference teachings. *Id.* Second, there must be a reasonable expectation of success. *Id.* Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *Id.* The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure. *Id.*

Claim 1 has been amended to include the element "through communications with the bufferless, non-blocking interconnecting network" and was previously amended to include the element "wherein the scheduling controller determines a maximal configuration of the bufferless, non-blocking interconnecting network and controls the configuration of the bufferless, non-blocking interconnecting network." These elements are fully support by the specification, including paragraph [0033] and [0034], which are reproduced below:

> [0033] Scheduling by scheduling controller 240 consists of two tasks: 1) scheduling the forwarding of cells from the N external input buffers (i.e., input ports 210) to the internal input buffers (i.e., input buffers 321-323); and (2) scheduling the switching of cells in internal input buffers 321-323 to internal output buffers 331-333. In principle, the CIOQ is controlled by the scheduling controller 240 to simulate an internally buffered crossbar (IBX). It is not required to be an exact simulation, but the delay discrepancy is tightly upper bounded by 2N slots. This can be done because, in a VOQ+IBX switch, there are at most T cells transmitted or received by an input or output port over any time interval of T slots.
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> [0034] FIG. 4 depicts flow chart 400, which illustrates the operation of exemplary packet switch 111 according to one embodiment of the present invention. During input scheduling, a cell is forwarded to the corresponding one of internal input buffers 321-323 if it would be forwarded to the an internally buffered crossbar (IBX) in the simulated switch (process step 405). During output scheduling, each cell is marked at its internal input buffer in the

> CIOQ as being active if it is selected by its destined output in the simulated switch to be transmitted out (process step 410). Switch 111 repeats steps 405 and 410 N times, once per time slot (process step 415). Next, switch 111 finds a maximal matching of inputs and outputs over all active cells currently queued at the internal input buffers of the CIOQ (process step 420). Switch 111 then configures bufferless crossbar 340 according to the current matching (process step 425) and transmits the matched head of line (HOL) cell at each VOQ (process step 430). Switch 111 then repeats step 420, 425 and 430 2N times, twice per time slot (i.e., speed-up of two) (process step 435). (Emphasis Added)

The Office Action asserted that the *Krishna* Arbiter (90) teaches the scheduling controller. The Office Action stated that *Krishna*, column 1, lines 22-30, discloses that the Arbiter (90) "controls the configuration of the bufferless, non-blocking interconnecting network." However, the Office Action argues that the *Krishna* switch fabric (89) (*Krishna*, col. 3, lines 63-65, col. 6, lines 60-61; channels 80-88) teaches the bufferless, non-blocking interconnecting network as recited in the claims of the instant application. However, as illustrated in *Krishna*, Figure 1, the arbiter (90) is not connected to the switch fabric (89) such that it can control the configuration of the switch fabric (89). Rather, the arbiter (90) is connected to the input ports (50), (51) and (52) and output ports (59), (60), and (61). Therefore, the Arbiter (90) cannot reasonably be interpreted as being "connected to the bufferless, non-blocking interconnecting network wherein the scheduling controller controls the configuration of the bufferless, non-blocking interconnecting network." However, in order to further prosecution, the Applicant has previously amended Claims 1, 4, 7 and 14 to recite "wherein the scheduling controller determines a maximal configuration of the bufferless, non-blocking interconnecting network and controls the configuration of the bufferless, non-blocking

interconnecting network."

The Applicant submits that Krishna does not teach or contemplate that the arbiter (90) could determine a maximal configuration of the bufferless, non-blocking interconnecting network.

Applicant further respectfully submits that the current application discloses a bufferless crossbar that is configurable. Krishna does not teach or contemplate a configurable bufferless crossbar. Krishna teaches a series of connections (Krishana, FIG. 1), but fails to disclose a crossbar that is configurable.

Krishna therefore fails to teach a *bufferless, non-blocking interconnection network*, as required by Claim 1 and its dependents, Claims 2 and 3. Similar arguments are true for Claim 4 (and its dependents, Claims 5 and 6), Claim 7 (and its dependents, Claims 8-13) and Claim 14 (and its dependents Claims 15-20).

In addition, each of the independent claims have been amended to include the element "based upon the data in the N input buffers." This element is respectfully submitted not to introduce any new matter, and it's entry is requested. This element is fully supported by the specification, as filed, including the following passages taken form pages 14 and 15 of the specification, as filed:

> Scheduling by scheduling controller 240 consists of two tasks: 1) scheduling the forwarding of cells from the N external input buffers (i.e., input ports 210) to the internal input buffers (i.e., input buffers 321-323); and (2) scheduling the switching of cells in internal input buffers 321-323 to internal output buffers 331-333. In principle, the CIOQ is controlled by the scheduling controller 240 to simulate an internally buffered crossbar (IBX). It is not required to be an exact simulation, but the delay discrepancy is tightly upper bounded by 2N slots. This can be done because, in a VOQ+IBX switch, there are at most T cells transmitted or received by an input or

> output port over any time interval of T slots.
>
> FIGURE 4 depicts flow chart 400, which illustrates the operation of exemplary packet switch 111 according to one embodiment of the present invention. During input scheduling, a cell is forwarded to the corresponding one of internal input buffers 321-323 if it would be forwarded to the an internally buffered crossbar (IBX) in the simulated switch (process step 405). During output scheduling, each cell is marked at its internal input buffer in the CIOQ as being active if it is selected by its destined output in the simulated switch to be transmitted out (process step 410). Switch 111 repeats steps 405 and 410 N times, once per time slot (process step 415). Next, switch 111 finds a maximal matching of inputs and outputs over all active cells currently queued at the internal input buffers of the CIOQ (process step 420). Switch 111 then configures bufferless crossbar 340 according to the current matching (process step 425) and transmits the matched head of line (HOL) cell at each VOQ (process step 430).

Moreover, there is no suggestion or motivation within *Krishna* to prompt one of ordinary skill to selectively combine discrete elements from *Krishna* and then *seek out* still others as required by the claims of the present application.

Accordingly, the Applicant respectfully requests that the § 103 rejection with respect to these claims be withdrawn.

CONCLUSION

As a result of the foregoing, the Applicant asserts that the remaining Claims in the Application are in condition for allowance, and respectfully requests an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***jmockler@munckcarter.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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